CLAIMS

1. A receiver comprising:

a filter that sends out an output signal having a symbol at an arbitrary time interval; and

an intermittent operation part that controls the filter intermittently at the time interval, according to the output signal supplied from the filter.

2. The receiver as claimed in claim 1, further comprising

a timing signal generator that generates a timing signal for turning on and off a power supply of the intermittent operation part, according to the arbitrary time interval in the output signal supplied from the filter.

3. The receiver as claimed in claim 2, wherein the timing signal generator generates a timing signal for turning on and off the power supply of the intermittent operation part, according to the control signal from the intermittent operation part.

4. The receiver as claimed in claim 2, wherein the timing signal generator generates a timing signal for turning on and off the power supply of the intermittent operation part, according to signal strength of the control signal from the intermittent operation part.

5. The receiver as claimed in one of claim 3 and claim 4, wherein the timing signal generator generates a timing signal for turning on and

off the power supply of the intermittent operation part, according to a control signal from the intermittent operation part and an off period of the power supply of the intermittent operation part.

6. The receiver as claimed in claim 1, further comprising a register that holds a control signal from the intermittent operation part, wherein the filter is controlled according to the control signal held by the register.

7. The receiver as claimed in claim 2, wherein the timing signal generator generates a timing signal for turning on and off the power supply of the intermittent operation part, according to a reference clock in addition to the arbitrary time interval in the output signal.

8. A frequency adjusting circuit including:

a reference filter that sets a phase difference to a reference clock signal;

a multiplication circuit that multiplies the output signal supplied from the reference filter by the reference clock signal; and

a low-pass filter that is connected to an output of the multiplication circuit, the frequency adjusting circuit providing the reference filter with an output voltage supplied from the low-pass filter, to provide the reference filter with negative feedback, so that a cutoff frequency of the reference filter remains constant, the frequency adjusting circuit comprising:

a sample hold circuit that holds an output voltage supplied from the low-pass filter for a constant period;

an analog-to-digital converter that converts an output voltage supplied from the sample hold circuit to digital data;

a digital-to-analog converter that converts the digital data to an analog adjusted value; and

a register that holds the digital data converted, wherein the frequency adjusting circuit is operated intermittently according to the digital data held by the register.

9. A frequency adjusting circuit including:

a reference filter that sets a phase difference to a reference clock signal; and

an XOR circuit that outputs an exclusive OR of the output signal supplied from the reference filter and the reference clock signal; and

a measurement circuit that measures a duty ratio of the output signal supplied from the XOR circuit, the frequency adjusting circuit using the output signal supplied from the measurement circuit for a control signal of the filter, the frequency adjusting circuit comprising a register that holds the output signal supplied from the measurement circuit as digital data, wherein the frequency adjusting circuit is intermittently operated.

10. An electronic device loaded with the receiver as claimed in claim 1.